WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising:

a plurality of data output pins;

a test pin;

a data processing circuit for generating output signals in response to input signals; and

an output circuit for outputting the output signals to the data output pins in a normal mode and sequentially outputting the output signals to the test pin in response to a clock signal in a test mode.

2. The integrated circuit of claim 1, wherein the output circuit controls the output signals not to be outputted to the data output pins in the test mode.

3. A semiconductor integrated circuit comprising:

a plurality of output pins;

a test pin;

a data processing circuit for generating output signals in response to input signals and transferring the generated output signals to the data output pins, and

an output circuit for sequentially outputting the output signals to the test pin in response to a clock signal.

4. The integrated circuit of claim 3, wherein the output circuit comprises a shift register operating in response to the clock signal.

5. A method for outputting data in a test mode of a semiconductor integrated circuit with a plurality of data output pins and a test pin, comprising:

determining whether the test mode is activated; and

sequentially outputting the output signals to the test pin in response to a clock signal in the test mode.

6. The method of claim 5, further comprising outputting the output signals to the data output pins if the test mode is not activated.